AMENDMENTS TO DRAWINGS:

The attached sheet(s) of drawings include changes to Figs. 2 and 5. These sheets replace the original sheets including Figs. 2 and 5.

In Figure 2, previously omitted reference characters D1 and D2 have been added in accordance with the specification, and as also shown in Fig. 5.

In Figure 5, previously omitted reference characters Cf1, Cf2, and Rf1 have been added in accordance with the specification.

REMARKS

Claims 1-22 are presented for consideration. Claims 1, 13, 14, 15, and 19 are currently amended. No claim is canceled.

The Specification is amended to address typographic and grammatical errors noted in the Office Action. Applicants thank the Examiner for noting these oversights.

The Abstract is amended to be not more than 150 words in length, as requested in the current Office Action.

Claim 1 is objected to for not using a colon mark ":" following the word "comprising". Applicants thank the Examiner, and have amended claim 1 accordingly.

Claim 13 is objected to because the recitation "if" in lines 23, 26, 29, and 33 is deemed to render the claim indefinite. The Office Action suggests changing the word "if" to "when". Claim 13 is amended accordingly.

Claim 14 is objected to for use of the word "if" for similar reasons as claim 13. Claim 14 is likewise amended to change the word "if" to "when", as suggested in the Office Action.

Claim 15 is objected to for use of the phrase, "i.e.", and it is suggested that this phrase be changed to "that is". Claim 15 is amended accordingly.

Claim 19 is objected to for using the word "if" in a manner similar to that of claim 13, and the Office Action suggest changing the word "if" to "when". Applicants again thank the Examiner, and have amended claim 19 accordingly.

Claims 13-22 are objected to as being dependent upon a rejected base claim, but would allowable if rewritten in independent form. Applicants thank the Examiner, and have rewritten claim 13 in independent form. It is noted that the limitation of claim 1 requiring that the bandwidth of the analog loop be greater than the bandwidth of said digital loop is not incorporated into currently amended claim 13 since the Office Action had indicated that this specific feature did not add to the patentability of the claim.

Claim 13 is believed to be in condition for allowance. Claims 14-22, which depend from claim 13 are likewise believed to be in condition for allowance based at least on the allowability of base claim 13.

Claims 1-4 and 11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Messerschmitt ("Frequency Detectors for PLL Acquisition in Timing and Carrier Recovery", IEEE Transaction on Communications, Publication Date: Sep 1979, Volume: 27, Issue: 9, pages: 1288-1295), hereinafter Messerschmitt.

Claims 5-10 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Messerschmitt as applied to claim 1, and further in view of Moon (U.S. Pat. 6,114,920) and Applicant's admitted Prior Art in page 5, lines 16-32 and page 11 line 31 to page 12, line 9.

Particularly in reference to Messerschmitt, the Office Action asserts that,

> " a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on the first and second control inputs (figure 1 "VCO", section page 1288)"

Applicants respectfully point out that Messerschmitt's Fig. 1 shows a VCO with only *one* control input. It is noted that Messerschmitt's Fig. 1 shows adding two control signal lines at a summing node to form a single VCO control signal line. It is also noted that in the specification of the present invention, Applicants provide multiple embodiments, including latter embodiments where a VCO having only one input and one output is used (see Figs. 4 and 5 of the present invention application). In the embodiments of Figs. 4 and 5, a summing node is used for combining two control inputs into a single control signal for a single-input VCO.

However, claim 1 reads more closely on the initial embodiments of Figs. 1 to 3 of the present invention. In these initial embodiments, a VCO that has two control inputs is used (see particularly Figs. 1 and Figs. 2). Fig. 1 clearly shows VCO 11 having an analogy input 11a and a digital input 11b. As is explained in

the specification, digital input 11b may be a signal bus comprised of multiple signal lines.

This is made more clear in Fig. 2, which shows an VCO with two separate control inputs. In Fig. 2, analogy control signal VCTL embodies a first (analog) control input, and Digital Control Bus 31 embodies a second (digital) control input. Analogy control input VCTL varies the frequency of VCO 11 by varying the capacitances of varactor pair D1/D2 (please see amended Fig. 2 for missing reference characters). Digital Control Input 31 varies the frequency of VCO 11 by individually turning ON/OFF selected transistors Mi to Mp to selectively insert or remove corresponding capacitors Ci to Cp from the oscillator circuit. Thus, first control input VCTL and second control input 31 provide separate and independent control of VCO 11 by separate and independent mechanisms.

The Specification further explains that digital control bus 31 may be generated by the circuit of Fig. 3. The point is that Figs. 1 and 2 clearly show a variable oscillator having a first control input and a second control input, as is required by claim 1, while Fig. 1 of Messerschmitt equally clearly shows a variable oscillator (VCO) having <u>one</u> control input and lacking a second control input. Thus, Applicants are at a loss for determining the relevance of the Messerschmitt VCO as applied to the present invention.

It should further be noted that a reason why this particular embodiment of the present invention can provide two separate control inputs to the VCO without creating instabilities is due a restriction relating the bandwidth of the analogy loop to the digital loop. This is stated, for example, at least in page 2, lines 28-35, wherein it states,

> "...The bandwidth of the digital loop is made much smaller than the bandwidth of analog loop. Preferably, the bandwidth of the analog loop is at least 200 times greater than the bandwidth of the digital loop. This gross parametric difference is used in the design of the VCO to allow two separate control inputs, a first analog control

> input provided by the PFD within the analog loop and a second digital control signal provided by the FDD within the digital loop. Both control inputs function relatively independently of each other."

Since Messerschmitt does not teach or suggest a VCO with two control inputs, it likewise does not teach or suggest that the bandwidth of the digital loop be made smaller than the bandwidth of the analogy loop.

However, the Office Action nonetheless asserts that Messerschmitt shows:

> "where the bandwidth of the analog loop is greater than the bandwidth of the digital loop (section 3.5 page 1292 end of first paragraph)."

Applicants respectfully point out the cited excerpt does not recite two separate loop frequency bandwidths. Rather, Messerschmitt is citing a difficulty in the technology by providing a statement regarding the general character of frequency offsets of general RF oscillators as compared to the typical bandwidth range of a carrier recovery loop.

Applicants contacted Examiner Torres to discuss this apparent misunderstanding. Examiner Torres agreed that the cited Messerschmitt did not address the claim limitation, but suggested that prior art of record U.S. Pat. 5,446,416 to Lin (hereinafter Lin) should be reviewed as it is the mostly likely to provide a discussion of bandwidth differences within a frequency synthesizer. Applicants thank Examiner Torres, and in accordance with his suggestion have studied the Lin reference.

Lin's prior art section discusses several types of dual-loop frequency synthesizer having a phase locking loop (PLL) and frequency locking loop (FLL). In the first examples, both the PLL and FLL appear to be analog, and in the later embodiment the PLL is analogy and the FLL to be digital. In discussion his prior art (Figs. 1 and 2) Lin notes that the two loops sum their control signals at a summation node (40 in Fig. 1; and 90 in Fig. 2) to create a single control signal to a common voltage controlled oscillator (VCO) (45 in Fig.

1 and 95 in Fig. 2), whose output is fed back to a phase detector and to a frequency detector. However, Lin explains due to both control signals being combined at summation node to create a single VCO control signal, the two loops becomes "highly inter-dependent", which introduces inter-loop interference that limits its operation (see for example col. 2, line 67 to col. 3, line 5).

Therefore, Lin proposes separating the loops by providing two separate VCOs (145 and 130, see Fig. 3) in two separate loops. Lin also replaces the digital frequency detector with a "frequency delimiter". As shown in Fig. 3, Lin's two loops do not share a common VCO, as is required by the present invention. Indeed, Lin teaches against such a structure.

Like in the present invention, Lin seeks to permit the two loops to function independent of each other, but Lin accomplishes it in a different manner. Firstly, as explained above, introduces a second VCO 130 solely for the loop housing the frequency delimiter 115. Secondly, Lin teaches that the frequency delimiter 115 should turn off when phase detector 125 is operational, and phase detector 125 should turn off when frequency delimiter 115 is operation. By having only one of the two loops operational at any given time, Lin can assure that the two loops remain independent of each other. Lin accomplishes this by incorporating a high-pass and a low-pass filter (Fig. 4) plus loop filter 135 (see Lin's col. 7, line 66 to col. 8, line 7). This results in the operational conditions shown in Lin's Fig. 5.

This, however, is different from the presently claimed invention. As noted above, Lin teaches against a dual loop system where both loops go though a single VCO. Furthermore, Line does not each or suggest a VCO having two control inputs, i.e. an analog control input and a digital control input. Rather, like Lin teaches the use of a summation node for combining two control signals into a common control signal for input to a VCO that has one control input and one control output. Also, line teaches against both loops operating at the same time.

Furthermore, Lin does not teach or suggest two loops each characterized by a different operational bandwidth, where one bandwidth is defined as being at least 200 times larger than the other. Rather, Lin teaches that one loop has a defined bandwidth, but the other loop does not have a defined bandwidth. The second loop has a two-part operational range defined as a first part from first undisclosed (starting) frequency up to a first cut-off frequency and a second part increasing from a second cut-off frequency up to a second undisclosed (ending) frequency. That is, Lin teaches that his PLL loop has an operational bandwidth defined as $-\Delta\omega_L$ to $+\Delta\omega_L$. However, Lin teaches that his FLL loop operates from a first undisclosed frequency up to first cut-off frequency $-\Delta\omega_L$, and operates from second cut-off frequency $+\Delta\omega_L$ up to a second undisclosed frequency.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration of the present application.

Respectfully submitted,

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